REMARKS

After entry of this amendment, claims 27-38, 40, and 42-44 will be pending in this application. Claims 21-26, 39, and 41 have been cancelled without prejudice. Claims 27, 31, and 38 have been amended. New claims 42-44 have been added. Support for the new and amended claims can be found in the specification. No new matter has been added.

Claims 27, 29-31, 33-34, 38, and 40 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kao et al., United States patent number 5,492,847. Claims 28, 35, 36, and 39 stand rejected under 35 U.S.C. § 103(a) as being anticipated by Kao et al. in view of Sanchez, United States patent number 5,583,067. Claim 37 stands rejected under 35 U.S.C. § 103(a) as being anticipated by Kao et al. in view of Sanchez, and further in view of Gilgen et al. Claims 27-34 and 38-40 stand rejected under 35 U.S.C. § 112, second paragraph. Reconsideration of the rejections and allowance of all the pending claims in light of the amendments and the following remarks is respectfully requested.

Formalities

Claims 27-34 and 38-40 stand rejected under 35 U.S.C. § 112, second paragraph. Applicants submit that these rejections have been obviated by amendment.

Drawings

The drawings were objected to as not showing every element of a claim 21. Since claim 21 has been cancelled without prejudice, applicants submit that the basis for this objection has been removed.

Claim 27

Claim 27 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Kao et al. But Kao et al. do not teach each and every element of this claim. For example,

claim 27 recites "wherein the first pocket implant and the second pocket implant are in contact at about the center of a channel region." Kao et al. do not teach this limitation.

In Figures 2A-2G, Kao teaches the use of APT pockets 232. But these pockets are not in contact at about the center of the channel region as required by the claim. Rather, the locations of these APT (anti-punch through) pockets are defined by the spacers 226, and are thus not in contact. Moreover, the APT pocket 432 in Figure 4 is a single pocket. It is not two pockets in contact with one another. (See Kao et al., column 7, lines 6-9.)

For at least these reasons, claim 27 should be allowed.

Claim 35

Claim 35 also stands rejected under 35 U.S.C. § 103(a) as being anticipated by Kao et al in view of Sanchez. But these references, even in combination, do not teach each and every element of this claim. For example, claim 35 recites "diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant." Neither Kao et al. nor Sanchez teach this limitation.

The pending office action states that Figure 4 of Kao et al. show that "the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing." (See office action mailed April 15, 2002, page 11, lines 1-3.)

But Kao et al. teach that APT implant 432 in Figure 4 is one implant, not two merged together. (See Kao et al., column 7, lines 6-9.) Accordingly, Kao et al. do not teach diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant as required by the claim. Sanchez adds nothing in regards to this element.

For at least these reasons, claim 35 should be allowed.

Claim 38

Claim 38 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Kao et al. But Kao et al. do not teach each and every element of this claim. For example, claim 38 recites "diffusing the first and second pocket implants laterally such that a threshold voltage of the transistor is increased." Kao et al. do not teach this limitation.

In fact, the only mention in Kao et al. regarding a threshold voltage appears in the background section. (See Kao et al., column 1, lines 29-34.) An increase in threshold voltage is cited as a detrimental result of a high concentration of well or substrate dopant in the prior art. Thus, Kao et al. teach away from diffusing the first and second pocket implants laterally such that a threshold voltage of the transistor is increased as required by the claim.

A transistor having such a higher threshold voltage provides an improved punch-through voltage, and is useful in applications such as voltage pumps and memory cell programming. Kao et al. do not provide this feature.

For at least these reasons, claim 38 should be allowed.

Other Claims

Claims 28-34 depend on claim 27, and should be allowed for at least the same reasons as claim 27, and for the additional limitations they recite.

Claims 36 and 37 depend on claim 35, and should be allowed for at least the same reasons as claim 35, and for the additional limitations they recite.

Claims 39 and 40 depend on claim 38, and should be allowed for at least the same reasons as claim 38, and for the additional limitations they recite.

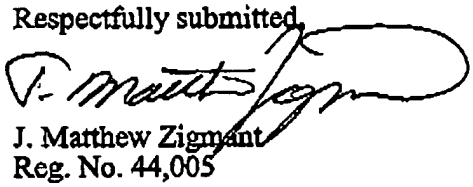
New claims 42-44 should be allowed for at least similar reasons as above, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,



J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: (415) 576-0300
JMZ:jmz
PA 3256961 v1

VERSION WITH MARKINGS TO SHOW CHANGES MADE

27. (Amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate; and

implanting a second pocket implant into the semiconductor substrate from a second side of the gate,

wherein **[the first pocket implant is near and separated by a small distance from the second pocket implant]** the first pocket implant and the second pocket implant are in contact at about the center of a channel region.

31. (Amended) The method of claim **[27]** 28 wherein the diffusing increases a reverse short channel effect of the transistor.

38. (Amended) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;

forming a gate oxide on the semiconductor substrate surface;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle; **[and]**

implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and **[,**

wherein a concentration of the pocket implants under the gate is nonuniform, and the pocket implants extend near the semiconduct r substrate surface]

diffusing the first and second pocket implants laterally such that a threshold voltage of the transistor is increased.